Cleanrooms
Oxidation of Si
Lithography
Ion Implantation
IBM’s Fishkill Fabrication Line
Running the Fab
Metallization and Etching cluster tool
Copper interconnects
Copper Interconnects
Processed Wafer

130 nm Cu-11 ASIC with PowerPC® processor and 1.0 GHz bus
Dicing
ASIC chip

IBM ASIC chip developed in CMOS 8S process technology.
Embedded DRAM ASIC

Embedded DRAM's greater density offers more memory on less silicon and less standby power needs than embedded SRAM, and a potentially smaller die size.
Si-Ge transistor
Si-Ge applications: high speed electronics on Si

Consumer Devices
One application of silicon germanium technology, which facilitates miniaturization of wireless products
Today's ever-increasing silicon integration means more is riding on each design — often including make-or-break business issues for your company. In a world where failure is not an option, 90 nm SoC design teams require methodologies and tools capable of handling the enormous capacity requirements, low power optimization, nanometer test challenges, and signal integrity issues intrinsic to these projects.

The Cadence Reference Flow for the IBM-Chartered 90 nm CMOS process streamlines the design of system-on-chip (SoC) devices with exceptional Quality of Silicon (QoS). By shortening the path from RTL to GDSII, this innovative, pre-tested approach, based on the Cadence Encounter digital IC design platform, is designed to enhance design team productivity and silicon reliability and to accelerate time-to-volume.

Reference Flow overview
The Cadence Reference Flow for the IBM-Chartered 90 nm CMOS process provides SoC developers with an optimized RTL-to-GDSII flow.

Based on the Cadence Encounter Platform, this advanced flow replaces traditional linear design flows with a completely new design strategy that can minimize time to wires and full chip iteration time to ensure the highest QoS. A nanometer router optimizes wire creation for performance and manufacturability, and a unified database has the capacity needed to support designs up to 50 million gates.

SoCs can be developed from floorplan through to silicon by the design team and/or by incorporating third-party IP validated with the flow.

The Quality-of-Silicon (QoS) metric
As SoC designs move towards 90 nm, new metrics for speed, area, power, and test are needed. QoS has emerged as the metric that exclusively handles measurements after wires. This new metric provides a mechanism for accurately measuring speed, area, and power offered by a netlist, and adds value at all stages of the design flow.

The capability to seamlessly integrate IP from multiple sources can lead to increased design efficiency and quicker time-to-silicon.
SOI Technology – 1.5-3 times more energy efficient and 33% better performance
Cell Microprocessor Briefing
February 7, 2005

Jim Kahle, IBM
Masakazu Suzuoki, Sony Computer Entertainment Inc.
Yoshio Masubuchi, Toshiba Corporation
Cell History

- IBM, SCEI/Sony, Toshiba Alliance formed in 2000
- Design Center opened in March 2001
- Based in Austin, Texas
- February 7, 2005: First technical disclosures
Cell
Cell Highlights

- Supercomputer on a chip
- Multi-core microprocessor (9 cores)
- >4 GHz clock frequency
- 10x performance for many applications
- Digital home to distributed computing
Introducing Cell

- Sets a new performance standard
  - Exploits parallelism while achieving high frequency
  - Supercomputer attributes with extreme floating point capabilities
  - Sustains high memory bandwidth with smart DMA controllers

- Designed for natural human interaction
  - Photo-realistic effects
  - Predictable real-time response
  - Virtualized resources for concurrent activities

- Designed for flexibility
  - Wide variety of application domains
  - Highly abstracted to highly exploitable programming models
  - Reconfigurable I/O interfaces
  - Autonomic power management
Microprocessor Architecture Trends

- GPU
- NIC
- Security
- Media

Hardwired Function

Programmable ASIC
- Streaming Graphics Processor
- Network Processor
- Security Processor
- Media Processor

Cell
- 64b Power Processor
- Synergistic Processor
- Config. IO

Synergistic Processor
Key Attributes

- **Cell is Multi-Core**
  - Contains 64-bit Power Architecture™
  - Contains 8 Synergistic Processor Elements (SPE)
- **Cell is a Flexible Architecture**
  - Multi-OS support (including Linux) with Virtualization technology
  - Path for OS, legacy apps, and software development
- **Cell is a Broadband Architecture**
  - SPE is RISC architecture with SIMD organization and Local Store
  - 128+ concurrent transactions to memory per processor
- **Cell is a Real-Time Architecture**
  - Resource allocation (for Bandwidth Measurement)
  - Locking Caches (via Replacement Management Tables)
- **Cell is a Security Enabled Architecture**
  - Isolatable SPE for flexible security programming
90nm SOI Technology

- 300mm fab
- 46nm Lpoly
- 1.05nm Tox
- Thick oxide (2.2nm) for analog, I/O
- Two $V_T$ settings for digital logic
- 1.0V nominal supply voltage
- 8 Levels Cu Metal + local interconnect
- Low k dielectric
Power Processor Element

- PPE handles operating system and control tasks
  - 64-bit Power Architecture™ with VMX
  - In-order, 2-way hardware Multi-threading
  - Coherent Load/Store with 32KB I & D L1 and 512KB L2
Synergistic Processor Element

- SPE provides computational performance
  - Dual issue, up to 16-way 128-bit SIMD
  - Dedicated resources: 128 128-bit RF, 256KB Local Store
  - Each can be dynamically configured to protect resources
  - Dedicated DMA engine: Up to 16 outstanding request
I/O and Memory Interfaces

- I/O Provides wide bandwidth
  - Dual XDR™ controller (25.6GB/s @ 3.2Gbps)
  - Two configurable interfaces (76.8GB/s @ 6.4Gbps)
  - Flexible Bandwidth between interfaces
  - Allows for multiple system configurations
Power Management

- Dynamic Power Management (DPM)
- Five Power Management States
- One linear sensor
- Ten digital thermal sensors
Element Interconnect Bus

- EIB data ring for internal communication
  - Four 16 byte data rings, supporting multiple transfers
  - 96B/cycle peak bandwidth
  - Over 100 outstanding requests
Results

Hardware Performance Measurement (85°C)

First pass hardware measurement in the Lab - Nominal Voltage = 1V
Interesting Statistics

- Observed clock speed: > 4 GHz
- Performance (single precision): > 256 GFlops
- Total # of transistors: 234M
- Total # of nets on chip: 1.4M
- Total # of repeaters on chip: 580K
- Simulation cycles: > 2 Trillion
- Extraction time on largest macro: 138 hrs
- Noise analysis on largest macro: 97 hrs
Displays

• Seeing is believing

  – Cathode ray tube (CRT)
  – Liquid Crystal Display (LCD)
  – Digital Light Projection (DLP)
  – Plasma Display
CRT resolution

• **Dot Pitch Explained:** Dot Pitch, or phosphor pitch, is a measurement indicating the diagonal distance between like-colored phosphor dots on a display screen. Measured in millimeters, the dot pitch is one of the principal characteristics that determines the quality of display monitors. The lower the number, the crisper the image. The dot pitch of color monitors for personal computers ranges from about 0.15 mm to 0.30 mm.
CRTs

• CRT Direct View/Rear Projection Advantages
  • Among the brightest and clearest alternatives
  • Excellent color and contrast potential
  • Relatively inexpensive
  • Excellent life expectancy
  • Heavy
  • Very deep
  • Analogue connectivity or D/A conversion of digital input connections
  • Potential for screen burn-in
CRT examples

- Mitsubishi WS-55813 Rear Projection CRT
- Sony KV34XBR910 Direct View CRT
LCD

- **LCD Display Advantages, Disadvantages**
- Good color reproduction
- Very thin
- Lightweight
- Perfect sharpness at native resolution
- Excellent longevity
- No screen burn-in effect
- Fixed resolution
- Notorious “screen door” effect on lesser models
- Poor contrast ratios (even excellent units have only 700:1)
- Very difficult to produce deep blacks (see above)
- Weak and “stuck” pixels are common
- Viewing angle on older models may be narrow
- Potential for slower refresh rates than plasma (some newer models are getting better)
LCD pixel concept

Electric current passes through the layer of liquid crystals

Shutters

Substrates

Light is prevented or allowed to pass through
LCD system geometries
LCD fabrication Process

- Deposition, Gate Metal (Ta, Al, MoTa)
- Patterning (1)
- Anode Oxidation (Ta$_2$O$_5$)
- Deposition [SiNx/a-Si(i)/SiNx]
- Patterning (2)
- Deposition (n + a-Si) for Electrode
- Patterning (3)
- Deposition, Source & Data Line (Ti, Al)
- Patterning (4)
- Deposition, Pixel Electrode (ITO)
- Patterning (5)
- Passivation
- Patterning

**Liquid Crystal Process**

<table>
<thead>
<tr>
<th>Sputter</th>
<th>Class 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class 100</td>
<td></td>
</tr>
</tbody>
</table>

**CVD**

- Clean
- Class 5000
- Etch

Proprietary Process
Defects in LCDs

<table>
<thead>
<tr>
<th>Composition</th>
<th>%</th>
<th>Composition</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array Process</td>
<td></td>
<td>Cell Process</td>
<td></td>
</tr>
<tr>
<td>Severed Signal Line</td>
<td>26.1</td>
<td>Point Defect*</td>
<td>32.6</td>
</tr>
<tr>
<td>Breakage</td>
<td>24.8</td>
<td>Dust, Scratches, Dirt*</td>
<td>24.7</td>
</tr>
<tr>
<td>Mo-Ta Etching Remnant*</td>
<td>23.0</td>
<td>Breakage</td>
<td>4.9</td>
</tr>
<tr>
<td>Faulty Characteristics</td>
<td>11.2</td>
<td>Line Defect*</td>
<td>7.7</td>
</tr>
<tr>
<td>Other</td>
<td>14.9</td>
<td>Faulty Gap*</td>
<td>6.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Other (i.e., unevenness)*</td>
<td>20.4</td>
</tr>
</tbody>
</table>

Source: Nikkei BP

* Indicates that dust is a factor. One half of the array defects and 90% of the cell process defects are linked to dust.
# Equipment Needed for LCD/TFT

<table>
<thead>
<tr>
<th>Process</th>
<th>Suppliers</th>
</tr>
</thead>
<tbody>
<tr>
<td>PECVD (Multichamber Batch)</td>
<td>Anelva, Shimadzu, Ulvac</td>
</tr>
<tr>
<td>Sputtering (Continuous Multichamber)</td>
<td>Anelva, Ulvac, Leybold, Shimadzu</td>
</tr>
<tr>
<td>Dry Etch (Single Substrate)</td>
<td>Anelva, Ulvac, Tokuda</td>
</tr>
<tr>
<td>Lithography (Cassette-to-Cassette)</td>
<td>Nikon, Canon, Dai Nippon Screen (MRS)</td>
</tr>
<tr>
<td>Wet Processing (Cleaning, Etching &amp; Resist Coating)</td>
<td>Dai Nippon Screen, Chuo Riken</td>
</tr>
</tbody>
</table>

---

**At Least:**

- 90 TFT-related manufacturing equipment suppliers
- 60 Test and inspection equipment suppliers
- 90 Materials suppliers - substrate, liquid crystal, polarizers, filters, etc.
Sputter Deposition Process
<table>
<thead>
<tr>
<th>Category</th>
<th>Cleaning Method</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>WET CLEANING</td>
<td>Brush Scrubbing</td>
<td>Removes stubborn particles; not suitable for smaller particles; effect is proportional to brushing pressure</td>
</tr>
<tr>
<td></td>
<td>Jet Spray</td>
<td>Suitable on patterned, hydrophilic, and soft surfaces; requires caution regarding static charge; ineffective without high water pressure</td>
</tr>
<tr>
<td></td>
<td>Ultrasonic Cavitation</td>
<td>Accelerating effect of chemical washing is conspicuous, has difficulty eliminating particles; requires caution regarding cleaning unevenness due to generation of standing waves</td>
</tr>
<tr>
<td></td>
<td>Megasonic (1 MHz)</td>
<td>Can eliminate submicron particles when used with chemical cleaning fluid; strong rectilinear propagation of sound waves; requires caution around jig structure</td>
</tr>
<tr>
<td>CHEMICAL CLEANING</td>
<td>Organic Solvent</td>
<td>Suitable for eliminating multiple contaminations of organic substances; solvent is chosen depending on contaminant; difficult with high level of cleaning</td>
</tr>
<tr>
<td></td>
<td>Neutral Detergent</td>
<td>Suitable for contamination from particles and organic substances; no damage to material being cleaned; difficulty is that interface activator adsorption layer remains</td>
</tr>
<tr>
<td></td>
<td>Chemical Cleaning Fluid</td>
<td>Depending on the orientation constituent, it acts in etching, oxide decomposition, hydrophilic surfaces, and ionization; suitable for all contaminants; needs chemical management</td>
</tr>
<tr>
<td></td>
<td>Pure Water</td>
<td>Eliminates chemicals after chemical processing; cleaning capability depends on water purity; insufficient for particles and organic substances</td>
</tr>
<tr>
<td>DRY CLEANING</td>
<td>Ultraviolet Ozone</td>
<td>Eliminates organic contaminants at the adsorption film level; improves coverage prior to resist application</td>
</tr>
<tr>
<td></td>
<td>Plasma Oxide</td>
<td>Applies to eliminating organic substances such as photoresist; not suitable for particles and nonorganic contaminants; lowthroughput</td>
</tr>
<tr>
<td></td>
<td>Non-oxide</td>
<td>Eliminates slight organic and inorganic contaminants; allows for highly clean surface; equipment is expensive; lowthroughput; limited application</td>
</tr>
<tr>
<td></td>
<td>Laser</td>
<td>Localized selective cleaning; not suitable for full surface cleaning</td>
</tr>
</tbody>
</table>
Comparing Sputtering and PECVD

<table>
<thead>
<tr>
<th></th>
<th>Sputtering</th>
<th>PECVD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deposition Rate</td>
<td>●</td>
<td>○</td>
</tr>
<tr>
<td>Film Thickness</td>
<td>●</td>
<td>○</td>
</tr>
<tr>
<td>Contamination</td>
<td>●</td>
<td>○</td>
</tr>
<tr>
<td>Mechanical Transfer</td>
<td>●</td>
<td>●</td>
</tr>
<tr>
<td>Heat/Cool Speed</td>
<td>●</td>
<td>○</td>
</tr>
<tr>
<td>Evacuate/Vent Speed</td>
<td>○</td>
<td>●</td>
</tr>
<tr>
<td>Substrate L/UL Speed</td>
<td>○</td>
<td>●</td>
</tr>
</tbody>
</table>

● = Much Influence
○ = Little Influence
More cleaning

<table>
<thead>
<tr>
<th>Process</th>
<th>Purpose</th>
<th>Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass Substrate</td>
<td>Particle Removal</td>
<td>Brush, Ultrasonic</td>
</tr>
<tr>
<td></td>
<td>Contaminants</td>
<td>Organic, Neutral Detergent</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Water</td>
</tr>
<tr>
<td>Before Deposition</td>
<td>Micro Crack</td>
<td>Chemical Etching</td>
</tr>
<tr>
<td></td>
<td>Particle</td>
<td>High Pressure Jet, Ultrasonic</td>
</tr>
<tr>
<td></td>
<td>Organic</td>
<td>Organic, Neutral Detergent</td>
</tr>
<tr>
<td></td>
<td>Inorganic</td>
<td>Water, Plasma</td>
</tr>
<tr>
<td></td>
<td>Surface Etch</td>
<td>Chemicals</td>
</tr>
<tr>
<td>Before Resist Coat</td>
<td>Particle</td>
<td>High Pressure Jet, Ultrasonic</td>
</tr>
<tr>
<td></td>
<td>Organic</td>
<td>UV/O3, Neutral Detergent</td>
</tr>
<tr>
<td></td>
<td>Inorganic</td>
<td>Water</td>
</tr>
<tr>
<td>After Resist RMV</td>
<td>Residuals</td>
<td>Chemicals</td>
</tr>
<tr>
<td></td>
<td>Resist Removal Material</td>
<td>Chemicals</td>
</tr>
<tr>
<td></td>
<td>Pattern Edge Correction</td>
<td>Chemicals</td>
</tr>
</tbody>
</table>
Too much cleaning?

<table>
<thead>
<tr>
<th>Features</th>
<th>Handling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Particle Size (µm)</td>
<td>Damage</td>
</tr>
<tr>
<td>Brush</td>
<td>&gt;10</td>
</tr>
<tr>
<td>Jet</td>
<td>&gt;5</td>
</tr>
<tr>
<td>US Cav.</td>
<td>&gt;3-5</td>
</tr>
<tr>
<td>US Vib.</td>
<td>&lt;3</td>
</tr>
</tbody>
</table>

Jet .......... High Pressure Water Jet
US Cav. .... Ultrasonic Cavitation
US Vib. .... Ultrasonic Vibration
# Packaging options

<table>
<thead>
<tr>
<th>Bonding configuration</th>
<th>Au bump</th>
<th>Sn/Pb bump</th>
<th>In alloy</th>
<th>Cu bump</th>
<th>Au ball</th>
<th>ACF</th>
<th>Conductive particle</th>
<th>Conductive particle</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Driver IC</strong></td>
<td>Pad</td>
<td>Solder</td>
<td>In alloy</td>
<td>Cu bump</td>
<td>Au ball</td>
<td>ACF</td>
<td>Al pad</td>
<td>Aupattern</td>
</tr>
<tr>
<td></td>
<td>IC</td>
<td></td>
<td>Metal</td>
<td>ITO</td>
<td>ITO</td>
<td>ITO</td>
<td>ITO</td>
<td>ITO</td>
</tr>
<tr>
<td><strong>Pitch</strong></td>
<td>100-300um</td>
<td>200-300um</td>
<td>50-150um</td>
<td>100-150um</td>
<td>60-130um</td>
<td>150-200um</td>
<td>&lt; 50um</td>
<td>60-130um</td>
</tr>
<tr>
<td><strong>LC panel</strong></td>
<td>ITO</td>
<td>Au</td>
<td>ITO</td>
<td>ITO</td>
<td>ITO</td>
<td>ITO</td>
<td>ITO</td>
<td>ITO</td>
</tr>
<tr>
<td><strong>Temp.</strong></td>
<td>RT</td>
<td>300-350°C</td>
<td>120-150°C</td>
<td>100-120°C</td>
<td>160-180°C</td>
<td>RT</td>
<td>150-200°C</td>
<td>RT</td>
</tr>
<tr>
<td><strong>Pressure</strong></td>
<td>&lt; 5 g/pad</td>
<td>&lt;20 g/pad</td>
<td>1-2 g/pad</td>
<td>&lt;50 g/pad</td>
<td>50-50 g/pad</td>
<td>10-10 g/pad</td>
<td>UV light</td>
<td>UV light</td>
</tr>
<tr>
<td><strong>Repeatability</strong></td>
<td>○</td>
<td>×</td>
<td>○</td>
<td>○</td>
<td>○</td>
<td>△</td>
<td>○</td>
<td>△</td>
</tr>
</tbody>
</table>
DLP (Digital Light Projection)

- DLP Advantages, Disadvantages
  - Incredible color reproduction
  - Excellent contrast ratios (using HD2+)
  - Lightweight
  - Excellent lamp life
  - Fully digital displays supporting DVI/HDMI without analogue conversion

- Requires a minimum of 12-14” depth for lamp-based technology
- Older models (pre-HD2) may not perform as well as upper scale CRT projection systems
- Potential for "Rainbow Effect" in older and single chip systems.
DLP principle
DLP system
DLP hardware
Plasma Displays

- **Plasma Advantages, Disadvantages**
  - Newer models have much better contrast ratios than many direct view TVs
  - Excellent color reproduction
  - Excellent life expectancy
  - Excellent viewing angle
  - Although thin, plasma TVs are fairly heavy (professional installation recommended for on-wall use)
  - Very susceptible to screen burn-in
  - Cannot produce deep black levels accurately
  - Fragile
  - Use a lot of power
Plasma light emission

1. A collision with a moving particle excites the atom.
2. This causes an electron to jump to a higher energy level.
3. The electron falls back to its original energy level, releasing the extra energy in the form of a light photon.
Plasma display cell
Plasma display concept
Matrix addressable Plasma cavities
Plasma display with coplanar plasma
Microwave Systems

ULQ-21 modules:
Waveform Generator (WG)
Polarization Modulator (PM)
100W Traveling Wave Tube Amplifier (TWTA)
Microwave Power Module (MPM)
2W Solid-State RF Amplifier (2W SSA)
Memory Modulator, I/J-Band (MM I/J-Band)
Memory Modulator, E/F-Band (MM E/F-Band)
Set-On Radar Receiver/Transmitter (RT)
Velocity Deception Amplifier (VDA)
Multiple Technique Deception Amplifier (MTDA)
Waveform-Controller Oscillator (WCO)
Command Interface Unit (CIU)
Frequency Translator (FT)
Range Gate Stealer Box (RGS Box)
Noise Generator
Traveling Wave Tube
Traveling Wave Tube Concept
Interaction between the electrons in the beam and the electromagnetic field generates bunches of electrons that in turn amplify the electromagnetic signal.

Note: The dimensions of the coil or cavity structure is optimized so that the microwave velocity matches the speed of the electrons in the e-beam.
Electron beam to Microwave Energy Transfer

RF input

Bunches of electrons

RF induced into helix
Micro-TWT
Slow-wave Geometries for TWT (other than coils)

Ring-loop structure

coupled-cavity structure

Ring-bar structure
TWT response compared to Solid State amplifier
Power consumption comparison
Noise comparison
Gain response of TWT
Traveling Wave Tube (TWT)

Carcinotron - opposite
Operation of Klystron

- One of the ways to generate high power microwaves, is through the use of a Klystron.
- The Klystron itself can be thought of as a small electron accelerator.

The Klystron operates by generating an electron beam at the cathode. These electrons are then accelerated by a DC power supply at the plate (anode). The velocity of the electrons is then modulated by an input signal. The electrons will drift towards the anode but due to the modulated velocity some will slow down and others will speed up. This will cause electron bunching at the output cavity, resulting in the excitation of a high-intensity microwave in the output cavity.
Klystron — invented by Russel and Sigurd Varian (Stanford)
Concept of Klystron

- Electrons are generated from a broad source (10kV)
- These electrons are introduced into a microwave cavity
- Microwave energy will bunch the electrons
- The electrons in turn generate electro-magnetic field that is coupled out (amplified signal)
- Electrons are dumped into collector
Reflex Klystron  (Sutton klystron)

- Electrons are launched into a microwave cavity, bunched and then forced back into that cavity by using a large electrostatic field on a repeller electrode.
Magnetron

The potential energy of an electron cloud is converted into r-f energy in a series of resonators

- The magnetron works by using a low-voltage alternating current and a high-voltage direct current. A transformer changes the incoming voltage to the required levels and a capacitor, in combination with a diode, filters out the high voltage and converts it to direct current. Inside the magnetron, electrons are emitted from a central terminal called a cathode. A positively charged anode surrounding the cathode and attracts the electrons. Instead of traveling in a straight line, permanent magnets force the electrons to take a circular path. As they pass by resonating cavities, they generate a continuous pulsating magnetic field, or electromagnetic(EM) radiation.

One way to generate microwaves is by the use of a Magnetron. Shown below is a typical magnetron that can be found in any household microwave oven.
Functions within a Magnetron

- Electrons are generated thermionically from a central emitter electrode.
- These are then accelerated towards the anode.
- A magnetic field makes the electrons go around in a circle.
- RF fields on the electromagnetic cavities on the spokes of the device can be used to accelerate or decelerate the electrons.
Electrons within the Magnetron

- Electrons are controlled by the RF field from the spokes
- Retarded electrons will curl towards the spokes, and accelerated electrons will curl away
- This generates electron cloud with spokes – each spoke is close to a resonator cavity with opposite field
- Field changes – electrons react
- The electrons map out the mode structure of the resonator cavity
Magnetron Cavity design

- Assuring that the magnetron maintains mode oscillation between specific modes is the goal of cavity design.
- Typically fewer than 20 resonator vanes are used.
- The physical size of each cavity is fixed to control the output frequency of the amplified signal.
- Cathode heat dissipation ultimately limits the power that can be generated.
- High-Q stabilizing cavities can be added to ensure the magnetron provides a stable frequency and stores energy (85%) away from main cavity – avoids arcing.
Thermal drift of Magnetron

- Electron bombardment heats up vanes
- Everything has to come to stable temperature
- This takes several minutes
YIG (Yttrium Iron Garnet) magnetically tuned filters

- 250-750 micron spheres are formed by tumbling

- Used for spectrum analyzers, tuning filters, etc.
- Example: 2-stage band rejection filter
MASER

• Hydrogen MASER