3. Overview of Microfabrication Techniques

The Si Revolution...

First Transistor
Bell Labs (1947)

Si integrated circuits
Texas Instruments (~1960)

Modern ICs

The Need of Micropatterning

The batch fabrication of microstructures requires a low-cost, high throughput surface patterning technology

Microfabrication Process

Complete processing sequence consist of:

- **Layering:**
  - Oxidation
  - Deposition

- **Patterning:**
  - Lithography
  - Etching

- **Doping:**
  - Ion Implantation
  - Diffusion

Robotics arm is used to transfer wafers

Check out: B. Van Zeghbroeck, "Principles of Semiconductor Devices"
W. Maly, "Atlas of IC Tech"
Again and Again…..

A typical process can have 15-20 masks

Bulk micromachining

Fabrication technologies for the machining of “bulk” microdevices in silicon

Example: Membrane Pressure Sensor

Example: MEMS Microturbines
3. Overview of Microfabrication...TOC

- Wafer-level Processes
  - Substrates
  - Wafer Cleaning
  - Oxidation
  - Doping
  - Thin-Film Deposition
  - Wafer Bonding

3. Overview of Microfabrication...TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization

3. Overview of Microfabrication...TOC

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Quartzite or SiO$_2$ (sand) is reacted in a furnace with carbon (from coke and/or coal) to make metallurgical grade silicon (MGS) which is about 98% pure, via the reaction:

\[
\text{SiO}_2 + 2\text{C} \rightarrow \text{Si} + 2\text{CO}
\]

The silicon is crushed and reacted with HCl (gas) to make trichlorosilane:

\[
\text{Si} + 3\text{HCl(gas)} \rightarrow \text{SiHCl}_3 + \text{H}_2
\]

Fractional distillation is then used to separate out the SiHCl$_3$ from most of the impurities. The (pure) trichlorosilane is then reacted with hydrogen gas to form pure electronic grade silicon (EGS):

\[
\text{SiHCl}_3 + \text{H}_2 \rightarrow 2\text{Si} + 3\text{HCl}
\]

The EGS is melted in a crucible, and then inserting a seed crystal on a rod called a puller which is then slowly removed from the melt.

If the temperature gradient of the melt is adjusted so that the melting/freezing temperature is just at the seed-melt interface, a continuous single crystal rod of silicon, called a boule, will grow as the puller is withdrawn.

The boule is grown down to a standard diameter. Flats are polished onto to boule to indicate crystalline orientation (above) before it is sliced into wafers.

- Substrates
- Wafer Cleaning
- Oxidation
- Doping
- Thin-Film Deposition
- Wafer Bonding
RCA cleaning of Si

The RCA cleaning procedure has three major steps used sequentially:

II. Oxide Strip: Removal of a thin silicon dioxide layer where metallic contaminants may accumulate as a result of (I), using a diluted 50:1 H₂O:HF solution.
III. Ionic Clean: Removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 H₂O:H₂O₂: HCl.

Thermal Oxidation

Thermal oxidation of silicon accomplished at high temperatures by flowing oxygen sources such as O₂ or H₂O

Thermal Oxidation (ctnd.)

Oxidation Reactions

\[ \text{Si (solid) + O}_2 \ (\text{gas}) \rightleftharpoons \text{SiO}_2 \ (\text{solid}) \]
\[ \text{Si (solid) + 2H}_2\text{O} \ (\text{gas}) \rightleftharpoons \text{SiO}_2 \ (\text{solid}) + 2\text{H}_2 \ (\text{gas}) \]

The growth of an oxide layer of thickness x will consume 0.44 x of silicon
Thermal Oxidation (ctnd.)

Horizontal Tube Furnace
Most popular furnace used for oxidation, diffusion, and heat treatments

Growth kinetics dictated by transport and diffusion of precursors at the Si/SiO₂ interface

3. Overview of Microfabrication...TOC

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The Silicon Lattice
The silicon atoms share valence electron through covalent bonds
**Conduction in Intrinsic Silicon**

At $T = 0 \text{ K}$, all covalent electrons are localized to their covalent bond, and therefore no conduction can take place.

At $T > 0 \text{ K}$ (above left), thermal agitation can be sufficient for some electrons to break away from the covalent bonds, and can freely drift around the lattice. These conduction electrons leave behind a "hole" in the covalent bond, which can also "move" by having nearby covalent electrons hop into the empty state. When a field is applied (above right), the conduction electrons drift in one direction, while the holes drift in the opposite ones.

**Band Structure: Intrinsic Material at $T > 0 \text{ K}$**

At $T > 0 \text{ K}$, thermal agitation can be sufficient for some electrons to break away from the covalent bonds, and can freely drift around the lattice. This will populate the conduction band with electrons, and the valence band with empty orbitals ("holes"), in equal amount ($n = p$).

**Doping of Semiconductors: n-type**

An impurity with extra valence electron releases this electron in lattice, therefore creating a surplus of electrons over holes ($n > p$).

**Doping of Semiconductors: p-type**

An impurity with less valence electrons creates a vacant state in the valence band, therefore creating a surplus of holes over electrons ($p > n$).
**Summary: Intrinsic vs Doped Material**

- **n-doped**
  - Material is rich in negatively charged conduction electrons
- **p-doped**
  - Material is rich in positively charged valence band holes

**Introduction of Dopants**

- **Local modification** of the material doping type and level
- Two methods are used:
  - Diffusion
  - Ion Implantation
- **Advantage of implantation:**
  - Less under-diffusion
  - Shallower junction
  - Better control of depth (energy)
  - Better control of concentration (dose)

**Doping by Diffusion**

- **Diffusion Process**
  - The diffusion process is ideally described in terms of Fick’s diffusion equation:
  
  \[
  \frac{\partial C}{\partial t} = D \frac{\partial^2 C}{\partial x^2}
  \]

  - Where \( C \) is the dopant concentration, \( D \) is the diffusion coefficient, \( t \) is time, and \( x \) is measured from the water surface in a direction perpendicular to the surface.

  - The initial conditions of the concentration \( C(0,t) = 0 \) at time \( t = 0 \) and the boundary conditions are that surface concentration \( C(0,t) = C_s \) (the solubility of the dopant) at surface and that a semi-infinite medium has \( C(\infty,t) = 0 \). The solution that satisfies the initial and boundary conditions is given by:

  \[
  C(x,t) = C_s \text{erfc} \left( \frac{x}{2\sqrt{Dt}} \right)
  \]

  - Where \( \text{erfc} \) is the complementary error function and the diffusion coefficient \( D \) is a function of temperature \( T \) expressed as:

  \[
  D = D_k \exp \left( \frac{-E_a}{kT} \right)
  \]

  - The total dose being diffused into semiconductor is:

  \[
  Q = \int_0^\infty C(x,t) \, dx = \frac{2C_s}{\sqrt{\pi}} \sqrt{Dt}
  \]

  - Where \( E_a \) is the activation energy of the thermally driven diffusion process, \( k \) is Boltzmann’s constant, and \( D \) is the diffusion constant.
Diffusion Process (ctnd.)

Figure 2.16 Theoretical diffusion profile of dopant atoms within a silicon wafer

Diffusion Process (ctnd.)

Figure 7-4 Solid solubility curves for various dopants in silicon. These values are the equilibrium solubilities at each temperature and may not be achieved in device-doped regions. (After [7.3].)

Numerical Example

Q: A p-type (boron) diffusion is performed in silicon as follows for 30 min at 900 °C. What is the deposited Q? Assume that the solid solubility is maintained at the surface (x=0)

Solution:
According to figures above, the boron diffusion coefficient is:

at 900 °C: \( D_{900}^{\infty} = 1.0 \exp \left( \frac{-3.5}{kT} \right) = 9.27 \times 10^{-10} \text{cm}^2 \text{s}^{-1} \)

The deposition is performed at 900 °C where the boron solid solubility from Table 7.4 is: \( C_s = 1.2 \times 10^{18} \text{cm}^{-3} \)

The dose introduced is then:

\[
Q = \frac{2C_s}{\sqrt{\pi}} \sqrt{Dt} = \frac{2(1.2 \times 10^{18})}{\sqrt{\pi}} \sqrt{\left(9.27 \times 10^{-10}\right)(30 \times 60)} = 1.75 \times 10^{14} \text{cm}^{-2}
\]
Doping by Ion Implantation

Allows precise control over dose and depth of doping layer

Doping profile controlled by implantation energy

Ion Implantation Process

The distribution is approximated at first order by a symmetric Gaussian distribution:

\[ C(x) = C_p \exp \left( \frac{(x - R_p)^2}{2\Delta R_p} \right) \]

where \( R_p \) is the average projected range normal to the surface, \( \Delta R_p \) is the standard deviation or straggle about that range, and \( C_p \) is the peak concentration where the Gaussian is centered. Range and standard deviation for common dopants in silicon are shown in next two slides. The total number of ions implanted is defined as the dose and is simply:

\[ Q = \int C(x) dx \]

Making use of the fact that the sum (or integral) of Gaussian functions is an error function, and using the formula which defines the error function gives

\[ \int \exp^{-u^2} du = \frac{\sqrt{\pi} \text{erf}(\infty) - \text{erf}(-\infty)}{2} \]

so that

\[ Q = \sqrt{2\pi} \Delta R_p C_p \]
Numerical Example

Q: Arsenic is implanted into a lightly doped p-type Si substrate at an energy of 75 keV. The dose is $1 \times 10^{14}$ cm$^{-2}$. The Si substrate is tilted 7° with respect to the ion beam to make it appear amorphous. The implanted region is assumed to be rapidly annealed so that complete electrical activation is achieved. What is the peak electron concentration produced?

A: From above graphs, the range and standard deviation for 75 keV arsenic are

$$R_p = 0.05 \mu m \quad \Delta R_p = 0.02 \mu m$$

The peak concentration is:

$$C_p = \frac{Q}{\sqrt{2\pi} \Delta R_p} = \frac{1 \times 10^{14}}{\sqrt{2\pi} (0.02 \times 10^{-4})} = 2 \times 10^{19} \text{ cm}^{-3}$$

Assuming all the dose is active, then the peak electron concentration is equal to the peak dopant concentration.
Channeling Effects

**Figure 8-10** Image of a silicon crystal looking down the 110 axial channels (top left), the 111 planar channels (top right), the 100 axial channels (lower left), and with a tilt and rotation to simulate a “random” direction (lower right).

Channeling Effects (ctnd.)

**Figure 8-11** Schematic of a channeling direction in silicon where an ion undergoes many small-angle reflections.

Channeling Effects (ctnd.)

**Figure 8-12** TSUPREM IV simulations [8.1] of boron profiles implanted into <100> crystalline silicon wafers with zero tilt and rotation. The implant energy is 35 keV. Note the deep channeling tails in crystalline silicon, which depend on the implant dose, in marked contrast with Figure 8-8 (after [8.4] and C.S. Rafferty [private communication].)

Ion implantation for production of buried oxide

- **02 Implant**
- **02 Implant**
- **02 Implant**

- **Anneal**

- Crystalline Si
- Stoichiometric SiO2
- Si with 02 implant
- Polysilicon
Cross-section of SIMOX wafers

(a) As implanted: 1.7E18/cm², 200keV, 520°C
(b) Annealed: 1320°C, 4hrs

SIMOX wafers for MEMS devices

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  - Wafer Bonding

Electronics Materials

Typical IC materials include:

- Thermal Oxides (covered previously)
- Other Dielectric Materials
- Polycrystalline silicon (Poly-Si)
- Metals
Electronics Materials

Typical IC materials include:

- Thermal Oxides (covered previously)
- Other Dielectric Materials
- Polycrystalline silicon (Poly-Si)
- Metals

Chemical Vapor Deposition

- SiO₂
  - Field oxide
  - interlevel insulator
  - passivation (overcoat layer)
- Si₃N₄
  - Local oxidation mask
  - protective overcoat layer
  - gate dielectric
- Poly-Si
  - gate material in MOSFET
- Metallization
  - interconnections
- Epitaxial layers
  - Si
  - Ge
  - GaAs
  - GaP

Purpose: Low temperature deposition of insulators & conductors

Check out: Plummer, Deal Griffin, Silicon VLSI Technology, Chap 9

Chemical Vapor Deposition (ctnd...)

A: Gaseous transport and adsorption of precursor
B: Surface transport and reaction
C: Desorption of by-products

For SiO₂:

SiH₄ + O₂ $\xrightarrow{900^\circ C}$ SiO₂ + 2H₂

SiCl₂H₂ + 2H₂O $\xrightarrow{900^\circ C}$ SiO₂ + 2H₂ + 2HCl

For Si₃N₄:

3SiCl₂H₂ + 4NH₃ $\xrightarrow{-80^\circ C}$ Si₃N₄ + 6HCl + 6H₂

For Poly-Si:

SiH₄ $\xrightarrow{600^\circ C}$ Si + 2H₂
**Low-Pressure CVD (LPCVD)**

1. Pressure between 0.2 and 2.0 torr
2. Gas flow between 1 to 10 cm³/s
3. Temperatures between 300 and 900 °C

**Plasma-Enhanced CVD (PECVD)**

Deposition of material physically assisted by RF plasma
Allows lower deposition temperatures

**Properties of Oxide Films**

<table>
<thead>
<tr>
<th>Property</th>
<th>Composition</th>
<th>Step coverage</th>
<th>Density ρ (g/cm³)</th>
<th>Refractive index n₀</th>
<th>Dielectric strength (V/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermally grown at 1000 °C</td>
<td>SiO₂</td>
<td></td>
<td>2.2</td>
<td>1.46</td>
<td>&gt;10⁻⁴</td>
</tr>
<tr>
<td>Deposited by SiH₄ + O₂ at 450 °C</td>
<td>SiO₂(H)</td>
<td>Nonconformal</td>
<td>2.1</td>
<td>1.44</td>
<td>8×10⁻⁶</td>
</tr>
<tr>
<td>Deposited by TEOS at 700 °C</td>
<td>SiO₂</td>
<td>Conformal</td>
<td>2.2</td>
<td>1.46</td>
<td>1×10⁻⁶</td>
</tr>
<tr>
<td>Deposited by SiCl₄H₂ + N₂O at 900 °C</td>
<td>SiO₂</td>
<td>Conformal</td>
<td>2.2</td>
<td>1.46</td>
<td>1×10⁻⁵</td>
</tr>
</tbody>
</table>

Ar atoms are ionized at low pressure by an electric field.
The positive ions are accelerated towards the negatively charged target:
Sputtered material condenses on the ambient surfaces
Electronics Materials

Typical IC materials include:

- Thermal Oxides
- Dielectric Materials
- Polycrystalline silicon (Poly-Si)
- Metals

Metallization

- Purpose: interconnecting the devices to form a circuit
- Use low resistance metal layers:
  - Aluminum alloys
  - Silicides
  - Copper
- Important issues:
  - resistivity
  - electromigration
  - planarity

Nine levels of metallization (with low-k dielectric and SiC-based barriers)

- Copper introduced in 2001 by IBM
- Lower resistance than Aluminum
- Less interconnection delays on chip
- Higher clock frequencies possible

(Source: AMD)

Check out: Plummer, Deal, Griffin, Silicon VLSI Technology, Chap 11

Metallization by Evaporation

3. Overview of Microfabrication...TOC

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Wafer bonding

- Used to permanently join two wafers together
- Allows the design and fabrication of multi-level devices assembled from the machining of separate wafers
- Fundamentals of process not fully understood, but does rely on formation of Si-O-Si bonds between wafers.

MEMS microturbines

Wafer bonding by fusion (ctnd.)

Fusion bonding procedures

1. Surface treatment to make hydrophilic surfaces by soaking wafers in Piranha, diluted sulfuric acid, or boiling nitric acid, or hydrophobic surfaces in HF. Hydrophilic top layer consisting of O-H bonds (hydroxyl) is formed on the oxide surface.

2. Contacting the wafers in clean air at room temperature after rinsing and drying them. Self-bonding (hydrogen bonding) is formed throughout the wafer surfaces without external pressure with considerable forces.

3. Annealing (> 800°C) in oxidizing or nonoxidizing ambient. Water molecules come out and the voids (intrinsic) are observed beyond 200°C. The voids tend to disappear and bonding strength is increased at more than 300°C forming siloxane (Si-O) bonds. At high temperatures (>800°C), Oxygen at the interface may diffuse into the silicon bulk to form Si-Si bonds like single crystal silicon at above 1000°C.
Wafer Bonding by Fusion

Thermal Considerations in Fusion Bonding

1. Temperature less than 450°C for postmetallisation wafers.
2. Temperature less than 800°C for wafers with diffusion dopant layers (e.g. p+ etch-stop layers).
3. Temperature greater than 1000°C for wafer bonding before processing. According to the reaction mechanism, annealing at temperatures above 1000°C for several hours should result in an almost complete reaction of the interface. A 1000°C anneal for about two hours gives sufficiently high bond strength for all subsequent treatments (Harendt et al. 1991); it is not possible to separate the two bonded Si wafers without breaking the silicon.

### Table 5.4  Bond quality data taken from Harendt et al. (1991)

<table>
<thead>
<tr>
<th>Structure</th>
<th>Annealing temperature (°C)</th>
<th>Bond strength (Jm⁻²)</th>
<th>Voids (% nonbonding)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/Si</td>
<td>450</td>
<td>0.5</td>
<td>–</td>
</tr>
<tr>
<td>Si/Si</td>
<td>800</td>
<td>0.6</td>
<td>0.3</td>
</tr>
<tr>
<td>Si/Si</td>
<td>1000</td>
<td>2.6</td>
<td>0.3</td>
</tr>
<tr>
<td>Si/Si₃N₄(140 nm)</td>
<td>800</td>
<td>0.9</td>
<td>0.2</td>
</tr>
<tr>
<td>Si/Si₃N₄(140 nm)</td>
<td>1000</td>
<td>Cleavage</td>
<td>0.2</td>
</tr>
<tr>
<td>Si/Si₃N₄(300 nm)</td>
<td>1000</td>
<td>Cleavage</td>
<td>25</td>
</tr>
</tbody>
</table>

Anodic Bonding: Principle

Anodic Bonding: Principle (ctnd.)
Anodic Bonding: Principle (ctnd.)

- Due to the elevated temperature, the Na+ ions are mobile enough for the Pyrex to behave like a conductor. Hence, in the very first moment, most of the voltage applied to the silicon-Pyrex sandwich drops across a small gap of a few microns between the two surfaces.

- The high electric field in this area creates a strong electrostatic force, pulling the two surfaces together and thus forming an intimate contact.

- In addition Na+ ions start drifting to the negative electrode, which is connected with glass, creating depletion zone adjacent to the silicon, positive electrode.

- During this charging process, the electric field is high enough to allow a drift of oxygen to the positive electrode (Si) reacting with silicon and creating Si-O bond.

Anodic Bonding Setup

Glass sputtered onto one of the silicon surfaces

Bonding take place at T ~300-400 °C, at V = 50 - 1200 V (greatly varies depending on glass used for bonding)

Anodic Bonding: Procedure

- Typical Variables: temperature, applied voltage, bonding load, voltage-applying time, bonding area, glass thickness. 300 – 400 °C, 700-1200V. (FYI: Temperature limit for IC processed Si substrates is about 450 °C)

- General conditions: Silicon + Pyrex 7740, 400 °C, and 1000V.

- Requirements:
  - Microroughness (Ra) < 1μm. Warp/bow < 5μm
  - The native or thermal oxide layer on the Si must be thinner than 2000Å.

- Benefits:
  - Lower temperature process and popular and reliable process
  - Less stringent requirement for the surface quality of the wafers.

Alternate Bonding Technique: Eutectic Bonding

One wafer coated with Au prior to bonding

Temperature is raised until the Eutectic point is reached

Above eutectic temperature, Au will diffuse into Si (and not other way around)

An Au-Si eutectic alloy is then formed between the two wafers

Other Si-metal alloys eutectic bonding also possible
Quality of bonds is usually monitored using infrared absorption imaging.

A better view of geometry of such device.
Worked example: Floating Element Shear Sensor

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Lithography
Lithography consists of patterning substrate by employing the interaction of beams of photons or particles with materials.

Photolithography is widely used in the integrated circuits (ICs) manufacturing.

The process of IC manufacturing consists of a series of 10-20 steps or more, called mask layers where layers of materials coated with resists are patterned then transferred onto the material layer.

A photolithography system consists of a light source, a mask, and an optical projection system.

Photoresists are radiation sensitive materials that usually consist of a photo-sensitive compound, a polymeric backbone, and a solvent.

Resists can be classified upon their solubility after exposure into: positive resists (solubility of exposed area increases) and negative resists (solubility of exposed area decreases).
Casting of Photoresists

Types of Photolithography

Resolution of Contact Lithography

Resolution of Projection Lithography

Contact lithography limited by Fresnel diffraction:

\[ W_{\text{lim}} = \sqrt{\lambda g} \]

where \( \lambda \) is wavelength employed and \( g \) is mask-resist gap.

Resolution and depth of focus of projection lithography limited by Rayleigh’s criterion:

\[ R = \frac{k_1 \lambda}{NA} \quad \text{DOF} = \pm \frac{k_1 \lambda}{(NA)^2} \]

where \( \lambda \) is wavelength employed, \( NA = \sin \alpha \), and \( k_1 \) is a constant (typically \( k_1 = 0.6 - 0.8 \)).
**Numerical Example**

Q: Estimate the resolution and depth of focus of a state-of-the-art excimer laser stepper using a KrF light source ($\lambda = 248$ nm) with a NA= 0.6. Assume $k_1 = 0.75$ and $k_2= 0.5$.

**Answer**

\[
R = k_1 \frac{\lambda}{NA} = 0.75 \left( \frac{248 \text{ nm}}{0.6} \right) = 0.31 \text{ nm}
\]

\[
\text{DOF} = \pm k_2 \frac{\lambda}{(NA)^2} = \pm 0.5 \left( \frac{248 \text{ nm}}{0.6} \right)^2 = \pm 0.34 \text{ nm}
\]

- Using additional technical "tricks" like off-axis illumination, the resolution can be pushed below 0.25 nm, suitable for the ITRS 0.25 μm generation.
- Further improvements can be obtained through more sophisticated mask designs using concepts like optical proximity correction and phase shift masks.
- The depth of focus is on the same order as the resist layer thickness itself and therefore requires very flat topography and careful attention in the stepper to keep the image plane focused by adjusting the height of the wafer with respect to the lens.

**Resolution Enhancement: Phase Shift Masks**

120 nm wide gates produced using $\lambda = 248$ nm radiation and PSM masks.

**Resolution of Photolithography (ctnd.)**

- Using additional technical "tricks" like off-axis illumination, the resolution can be pushed below 0.25 nm, suitable for the ITRS 0.25 μm generation.
- Further improvements can be obtained through more sophisticated mask designs using concepts like optical proximity correction and phase shift masks.
- The depth of focus is on the same order as the resist layer thickness itself and therefore requires very flat topography and careful attention in the stepper to keep the image plane focused by adjusting the height of the wafer with respect to the lens.

**EUV Lithography System...**

One in every home...
Alternate Nanolithography Techniques

- Micro-contact Printing
- Nanoimprint Lithography
- Scanned Probe Lithography
- Dip-pen Lithography

Micro-Contact Printing

1) Application of ink to stamp
2) Application of stamp to surface
3) Removal of stamp
4) Residues rinsed off

Source: IBM Zurich

Micro-Contact Printing (ctnd.)

Printing of PDMS

Source: Winograd Group, Penn State

Selective Growth of Neurons on Printed Surfaces

Biological interactions that underlie neuron cell attachment and growth are being employed to produce defined networks of neurons.

Microcontact printing has been used to place chemical, biochemical, and/or topographical cues at designated locations.

Important potential for the interfacing of solid state electronics with nerve cell biology, and for the fundamental electrical studies of single nerve cells.

Source: Craighead Group, Cornell

Selectivity growth of neurons on chemically patterned Si (C. D. James et al.)
Alternate Nanolithography Techniques

- Micro-contact Printing
- Nanoimprint Lithography
- Scanned Probe Lithography
- Dip-pen Lithography

Nanoimprint Lithography

Consists of pressing a mold onto the resist above its glass transition temperature $T_g$

More? Check out S. Y. Chou, Princeton

NIL Master

- SiO$_2$ pillars with 10 nm diameter, 40 nm spacing, and 60 nm height fabricated by e-beam lithography.
- Master can be used tens of times without degradation

NIL Pattern in PMMA

- Mask is pressed into 80 nm thick layer of PMMA on Si substrate at 175° C ($T_g=105 \degree$ C), P= 4.4 MPa.
- PMMA conforms to master patterning, resulting in ~10 nm range holes
**Alternate Nanolithography Techniques**

- Micro-contact Printing
- Nanoimprint Lithography
- Scanned Probe Lithography
- Dip-pen Lithography

**Scanned Probe Lithography**

Source: Quate Group, Stanford

**Fabrication of CMOS Gate Using SPM Lithography**

Source: Quate Group, Stanford

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Need for Etching Processes

- Selective removal of material as defined by photolithography

Isotropic vs. Anisotropic Etching

- More Directional Etching

(a) Isotropic
(b) Anisotropic
(c) Completely Anisotropic
Selectivity of Etch Process

(a) 

(b) 

Isotropic vs anisotropic etching: etching bias
- Bias = d_f - d_m
- Complete isotropic etching B=2h_f
- Complete anisotropic etching B=0

Degree of anisotropy

\[ A_f = 1 - \frac{|B|}{2h_f} \]

0 ≤ A_f ≤ 1

• A_f = 0: isotropic \[ |B| = 2h_f \]

• A_f = 1: anisotropic \[ |B| = 0 \]

Wet Etching of Si

Etching of Si:

\[ Si + 2H^+ \rightarrow Si^{2+} + H_2 \]

\[ SiCl_n \text{ (absorbed) } \rightarrow SiCl_n \text{ (gas) } \]
Anisotropic etchants in silicon

\[ w = w_0 - 2h \coth(55^\circ) \]

**Figure 5.1** Anisotropic etching of (100) crystal silicon

<table>
<thead>
<tr>
<th>Table 5.1</th>
<th>Anisotropic etching characteristics of different wet etchants for single-crystalline silicon</th>
</tr>
</thead>
<tbody>
<tr>
<td>Etchant</td>
<td>Temperature (°C)</td>
</tr>
<tr>
<td>KOH:H₂O</td>
<td>80</td>
</tr>
<tr>
<td>KOH</td>
<td>75</td>
</tr>
<tr>
<td>EDP</td>
<td>110</td>
</tr>
<tr>
<td>N₂H₄H₂O</td>
<td>118</td>
</tr>
<tr>
<td>NH₄OH</td>
<td>75</td>
</tr>
</tbody>
</table>

**KOH etch of Si**
- KOH etches silicon substrate
  - V-grooves, trenches
  - Concave stop, convex undercut
  - (100) to (111) → 100 to 1 etch rate
- Masks:
  - SiO₂: for short period
  - Si₃N₄: Excellent
  - heavily doped P⁺⁺ silicon: etch stop

**Example MEMS Velcro**
Example: MEMS Velcro (ctnd.)

Need for etch-stopping layers

Wet Etching of Other Materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Etchant</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>HF (49%, in water)</td>
<td>Selective over Si (i.e., will etch Si very slowly in comparison). Etch rate depends on film density, doping. About 1/3 the etch rate of straight HF. Etch rate depends on film density, doping. Will not lift up photoresist like straight HF.</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>HF (49%)</td>
<td>Etch rate depends strongly on film density. O₂ in film. Selective over SiO₂. Requires oxide mask.</td>
</tr>
<tr>
<td>Al</td>
<td>H₂PO₄:H₂O (boiling at 130-180°C)</td>
<td>Selective over Si, SiO₂, and photoresist.</td>
</tr>
<tr>
<td>Poly-Si</td>
<td>HNO₃:H₂O:H₂O₂ (+ CH₃COOH) (1:1:2)</td>
<td>Etch rate depends on etchant composition.</td>
</tr>
<tr>
<td>Single-crystal Si</td>
<td>HNO₃:H₂O:H₂O₂ (+ CH₃COOH) (5:2:2:2)</td>
<td>Etch rate depends on etchant composition.</td>
</tr>
<tr>
<td>KOH:IPA</td>
<td>(13 wt. % KOH, 13 wt. % IPA)</td>
<td>Crystallographically selective; relative etch rates (100:100:1): 1</td>
</tr>
<tr>
<td>Ti</td>
<td>NH₄OH:H₂O₂:H₂O (1:1:5)</td>
<td>Selective over TSi;</td>
</tr>
<tr>
<td>TiN</td>
<td>NH₄OH:H₂O₂:H₂O (1:1:5)</td>
<td>Selective over TSi;</td>
</tr>
<tr>
<td>TSi</td>
<td>NH₄OH:H₂O₂:H₂O (6:6:1)</td>
<td>Selective over TSi;</td>
</tr>
<tr>
<td>Photoresist</td>
<td>HSO₃:H₂O (12°C)</td>
<td>Organic strippers For wafers without metal.</td>
</tr>
</tbody>
</table>

Need for etch-stopping layers (ctnd.)
**Doping-selective etching (ctnd.)**

Table 5.2 Dopant-dependent etch rates of selected silicon wet etchants

<table>
<thead>
<tr>
<th>Etchant (Diluent)</th>
<th>Temperature (°C)</th>
<th>(100) Etch rate (µm/min) for boron doping ≤ 10^{19} cm^{-3}</th>
<th>Etch rate (µm/min) for boron-doping ≥ 10^{20} cm^{-3}</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDP (H_{2}O)</td>
<td>115</td>
<td>0.75</td>
<td>0.015</td>
</tr>
<tr>
<td>KOH (H_{2}O)</td>
<td>85</td>
<td>1.4</td>
<td>0.07</td>
</tr>
<tr>
<td>NaOH (H_{2}O)</td>
<td>65</td>
<td>0.25–1.0</td>
<td>0.025–0.1</td>
</tr>
</tbody>
</table>

- Disadvantage: requires high-dopant concentration to achieve good selectivity

**Electrochemical etching**

Steps:
1. Injection of holes into the semiconductor to raise it to a higher oxidation state Si⁺
2. Attachment of negatively charged hydroxyl groups, OH⁻, to the positively charged Si
3. Reaction of the hydrated silicon with the complexing agent in the solution
4. Dissolution of the reaction products into the etchant solution

**Electrochemical etching (ctnd.)**

Plot of electrochemical current density against voltage for silicon doped to different resistivities
Electrochemical etch stop (ctnd.)

- Current-voltage characteristics of n-Si and p-Si in KOH. No current flows at the OCP and the current stops above the passivating potential.

Example #1: fabrication of membranes

- Method to fabricate an array of thin membranes: (a) design of an oxide mask and (b) the electrochemical cell providing a back etch.

Example #2: fabrication of cantilevers

- Oxidation and patterning (a)
- Diffusion of phosphorus (b)
- Removal of the oxide (c)
- Selective p/n etching (d)

Figure 5.15  Process flow of diffused pattern technique

Example #2: fabrication of cantilevers (ctnd.)

- Diffusion of phosphorus (a)
- Oxidation and patterning (b)
- Anisotropic etching through n-layer (c)
- Selective p/n etching (d)

Figure 5.16  Process flow of etched-pattern technique
3. Overview of Microfabrication...TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization

Dry Etching Methods

Dry etching required for small feature size:
- Anisotropic
- High aspect ratios

Types:
- Reactive Ion etching (right)
- Sputtering
- Ion beam milling

Check out: Plummer, Deal Griffin, Silicon VLSI Technology, Chap 10

Plasma Etching

![Schematic diagram of an RF-powered plasma etch system.](image)

Plasma Induced Etching Processes

- Dissociation:
  - $\text{CF}_4 + e^- \rightarrow \text{CF}_3 + F + 2e^-$
- Ionization:
  - $\text{CF}_3 + e^- \rightarrow \text{CF}_3^+ + 2e^-$
- Excitation:
  - $\text{CF}_4 + e^- \rightarrow \text{CF}_4^+ + e^-$
- Dissociative ionization:
  - $\text{CF}_4 + F + e^- \rightarrow \text{CF}_3^+ + F + 2e^-$
- Recombination:
  - $\text{CF}_3^+ + F + e^- \rightarrow \text{CF}_4$
  - $F + F \rightarrow F_2$
Plasma Induced Etching Processes (ctnd)

Etchant (Free Radical) Creation
\[ e^- + O_2 \rightarrow O \]

- Etchant Transfer
- Byproduct Removal

Etched Structures

- Advantages:
  - Good directional etching
  - Good selectivity: SiO\(_2\) to Si (35:1)

SCREAM process overview

SCREAM process overview (ctnd.)
3. Overview of Microfabrication...TOC

- Pattern Transfer
  - Optical Lithography
  - Design Rules
  - Mask Making
  - Wet Etching
  - Dry-Etching
  - Lift-Off
  - Planarization

Transfer by lift-off process

- Optical Lithography
- Design Rules
- Mask Making
- Wet Etching
- Dry-Etching
- Lift-Off
- Planarization (read)